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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/605,607	10/13/2003	Herbert L. Ho	FIS920030214US1	2606

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EXAMINER	
CHEN, ERIC BRICE	
ART UNIT	**PAPER NUMBER**
1765	

DATE MAILED: 07/12/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/605,607	HO ET AL.	
	Examiner	Art Unit	
	Eric B. Chen	1765	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 5/2/05.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-18 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-18 is/are rejected.

7)☒ Claim(s) 2-3 and 11-12 is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 1 and 10 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The phrase "a depth corresponding to a desirable deep trench depth" in claims 1 and 10 is a relative term which renders the claim indefinite. The language is subjective and has multiple interpretations regarding the depth of the trench.

3. Claims 2-9 are rejected under 35 U.S.C. 112, second paragraph, because they are dependent on indefinite base claim 1.

4. Claims 11-18 are rejected under 35 U.S.C. 112, second paragraph, because they are dependent on indefinite base claim 10.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1 and 10 stand rejected under 35 U.S.C. 102(b) as being anticipated by Kleinhenz (U.S. Patent No. 5,770,484).

7. As to claim 1, Kleinhenz discloses a method for etching a silicon on insulator (SOI) substrate, the method comprising: opening (column 4, lines 12-15) a hardmask layer (130/140/150) (column 3, lines 66-67; column 4, lines 1-9) formed on an SOI layer (120) of the SOI substrate (100/110) (column 3, lines 40-42); etching through said SOI layer (120), a buried insulator layer (110) underneath said SOI layer, and a bulk silicon layer (100) beneath said insulator layer a single etch step, wherein said single etch step is sufficient to etch through said bulk silicon layer to a depth corresponding to a desirable deep trench depth (column 4, lines 12-22; Figure 4).

8. . As to claim 10, Kleinhenz discloses a method for forming a deep trench within a silicon on insulator (SOI) substrate, the method comprising: forming a hardmask layer (130/140/150) (column 3, lines 66-67; column 4, lines 1-9) on an SOI layer (120) of the SOI substrate (100/110) (column 3, lines 40-42); patterning a desired deep trench pattern in said maskmask layer (column 4, lines 12-15; Figure 4); and etching through said SOI layer (120), a buried oxide (BOX) layer (110) underneath said SOI layer, and a bulk silicon layer (100) beneath said BOX layer using a single etch step, wherein said single etch step is sufficient to etch through said bulk silicon layer to a depth corresponding to a desirable deep trench depth (column 4, lines 12-22; Figure 4).

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims 4 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kleinhenz, in view of Rossnagel et al., *Handbook of Plasma Processing*, Noyes Publications (1990).

11. As to claim 4 and 13, Kleinhenz does not expressly disclose that the etching is implemented at a pressure of about 10 to about 150 mTorr. However, Rossnegal summarizes the typical characteristics for plasma etching (Table 1, page 198), including a gas pressure of 10-200 mTorr. It should be noted that Applicants' claimed gas pressure falls within the conventional ranges taught by Rossnegal. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to select a gas pressure range of about 10 to about 150 mTorr. One of ordinary skill in the art would have been motivated to select this range, because it is known to successfully accomplish plasma etching.

12. Claims 5 and 14 rejected under 35 U.S.C. 103(a) as being unpatentable over Kleinhenz, in view of Wolf, *Silicon Processing for the VLSI Era*, Vols. 1 and 4, Lattice Press (1986, 2002).

13. As to claims 5 and 14, Kleinhenz does not expressly disclose that the hardmask layer is formed at a thickness so as to accommodate a 1:1 etch selectivity with respect to said buried insulator layer and selectivity with respect about a 5:1 to about a 35:1 etch to said SOI layer and said bulk silicon layer. Wolf teaches that both the mask material and underlying layer materials are generally etchable and that selectivity is the ratio of the of etch rates of different materials. Etch selectivity with respect to the mask material plays a role in the etched size features. Wolf also teaches that overall film thickness (or depth of an etched feature) influences etch selectivity (vol. 1, page 523), such that etching a thicker film (or deeper feature) requires a thicker etch mask (vol. 1, page 524, Figure 7). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include the step of forming the hardmask layer at a thickness so as to accommodate a 1:1 etch selectivity with respect to said buried insulator layer and selectivity with respect about a 5:1 to about a 35:1 etch to said SOI layer and said bulk silicon layer. One who is skilled in the art would be motivated to form a hardmask layer of appropriate thickness, such that the hardmask layer is not completely removed by etching, prior to etching a feature to its desired depth.

14. Claims 6-8 and 15-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kleinhenz, in view of Wolf, in further view of Sell (U.S. Patent App. Pub. No. 2004/0147074).

15. As to claims 6 and 15, Kleinhenz does not expressly disclose that said hardmask layer further comprises: a pad nitride layer formed on said SOI layer; and a borosilicate

glass (BSG) oxide layer formed on said pad nitride layer. However, Sell discloses a DRAM hardmask structure, including a pad nitride layer (44) formed on said SOI layer (47); and a borosilicate glass (BSG) oxide layer formed on said pad nitride layer (paragraph 0076; Figure 8). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use a hardmask layer further comprising: a pad nitride layer formed on said SOI layer; and a borosilicate glass (BSG) oxide layer formed on said pad nitride layer. One who is skilled in the art would be motivated to form a hard mask structure similar to one that is conventional or one that has been used to successfully produce a DRAM device, because such a hard mask structure is known to protect underlying layers during etching.

16. As to claims 7 and 16, Sell discloses that the hardmask layer is formed at a thickness of about 6,000 Å to about 20,000 Å (paragraph 0076). The total thickness of the hardmask layer is the total thickness of layers (44) and BSG layer. Layer (44) is 200 nm thick; BSG layer is 1,000 nm thick. The total thickness of the hardmask is 1,200 nm (12,000 Å).

17. As to claims 8 and 17, Sell discloses that the hardmask layer is formed at a thickness of about 10,000 Å to about 18,000 Å (paragraph 0076).

18. Claims 9 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kleinhenz, in view of Wolf, in further view of Sell.

19. As to claims 9 and 18, Kleinhenz does not expressly disclose that the BOX layer is formed at a thickness of about 120 to about 140 nanometers. However, Wolf teaches that for silicon-on-insulator technology, a typical range for the thickness of the BOX

layer is 90-150 nm (vol. 4, pages 535-36). It should be noted that applicants' claimed BOX thickness falls within the conventional thickness range taught by Wolf. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to select a BOX thickness of about 120 to about 140 nanometers. One of ordinary skill in the art would have been motivated to select this conventional thickness range, because it is known to successfully produce a silicon-on-insulator device.

Allowable Subject Matter

20. Claims 2-3 and 11-12 would be allowable if rewritten or amended to overcome the rejection under 35 U.S.C. 112, second paragraph, set forth in this Office action.

21. Claims 2-3 and 11-12 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

22. The following is a statement of reasons for the indication of allowable subject matter for claims 2 and 11: the prior art fails to teach or suggest that etching is implemented with an HBr, NF_3 and O_2 etch chemistry. The closest prior art, Sell, discloses etching through said SOI layer (47), and a bulk silicon layer (41) beneath said BOX layer (paragraph 0076; Figure 9) using an HBr, NF_3 and O_2 etch chemistry. Sell further discloses etching through a buried oxide (BOX) layer (46) underneath said SOI layer with an CHF_3/O_2 chemistry. However, there is no motivation of suggestion of etching buried oxide (BOX) layer (46) underneath said SOI layer with an HBr, NF_3 and O_2 etch chemistry.

Response to Arguments

23. Applicants' arguments (Applicants' Remarks, pages 5-6), filed May 2, 2005, regarding the rejection of claims 1 and 10 under 35 U.S.C. 102(b) as being anticipated by Kleinhenz have been fully considered but they are not persuasive. Applicants' amended language, "a depth corresponding to a desirable deep trench depth" is subjective and has multiple interpretations regarding the depth of the trench. Therefore, claims 1 and 10 remain anticipated by Kleinhenz.

24. Applicants' arguments (Applicants' Remarks, pages 5-6), filed May 2, 2005, regarding the rejection of claims 1-2 and 11-12 under 35 U.S.C. 102(e) as being anticipated by Sell have been fully considered and are persuasive. Applicants have correctly pointed out that the Sell reference fails to teach the element of "implementing a *single* etch step to etch through an SOI layer, a buried oxide layer underneath the SOI layer, and a bulk silicon layer (emphasis added)" (Applicants' Remarks, pages 6-7). Therefore, the rejection has been withdrawn.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric B. Chen whose telephone number is (571) 272-2947. The examiner can normally be reached on Monday through Friday, 8AM to 4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nadine G. Norton can be reached on (571) 272-1465. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

EBC

EBC
June 27, 2005

NADINE G. NORTON
SUPERVISORY PATENT EXAMINER